

LNF - 64/17
18 Maggio 1964.

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ABSTRACT

The functional elements that belong to an automatic pulse selection and registration unit with dead time less than 10 ns, particularly suited for nuclear physics experiments with high flux of particles from accelerating machines, will be described.

They are:

- a) Fast coincidence circuitry with anticoincidence, resolving time less than 2 ns.
- b) Current linear gate, linearity better than 1% for pulses from 1 mA to 20 mA amplitude.

INTRODUCTION

We will describe two circuits belonging to a 100 megapulses/sec unit⁽¹⁾, that is under development in our laboratories for fast nucleonic instrumentation.

To achieve high speed, we based our work on the following ideas: d. c. coupling, low input and output impedances, current operation, pulses injected to earth for both input and output of each module. Maximum linear output is 20 mA.

We have basically assumed the tunnel diode and common-base transistor coupling technique, in accordance to the ideas of Amodei and Kosonocky⁽²⁾, to combine high speed current-switching of an unilateral common-base transistor with the bistable character, high speed switching

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and current gain of a tunnel diode.

COINCIDENCE CIRCUIT.

The circuit has fourfold coincidence inputs plus an anticoincidence one. The complete schematic is shown in Fig. 1.

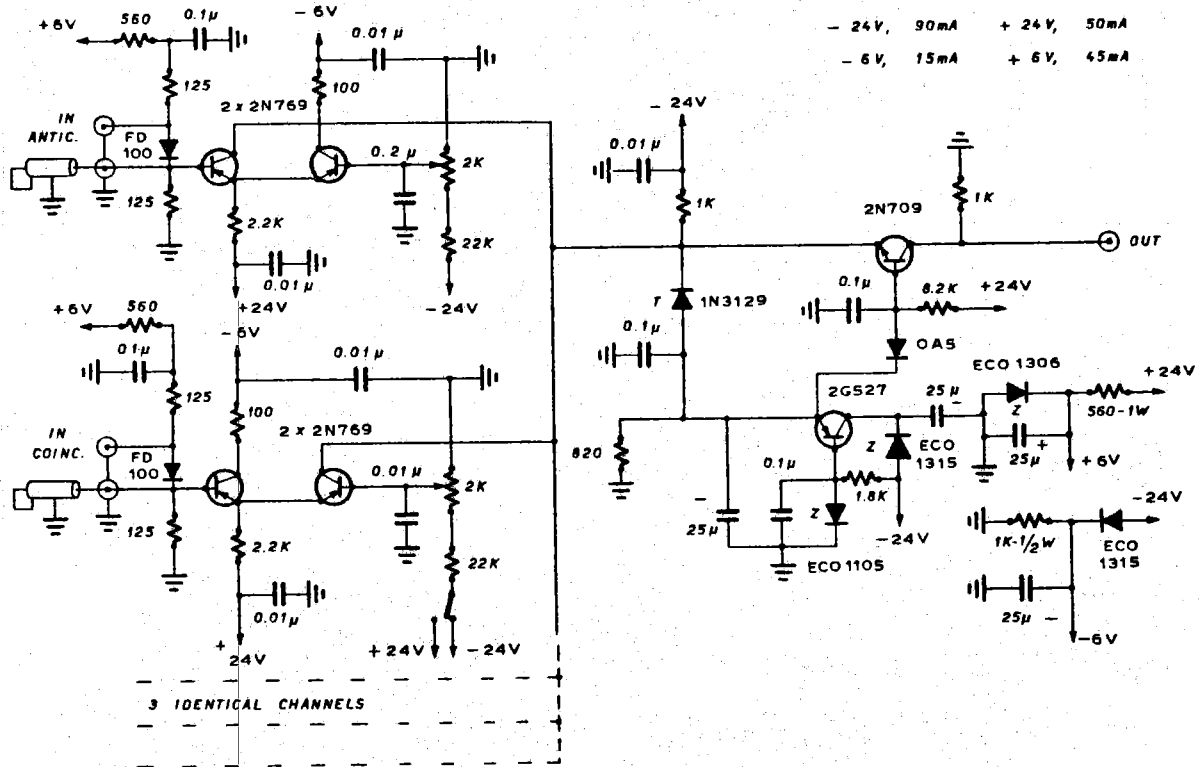


FIG. 1 - Coincidence circuit complete schematic.

Both the four "yes" and the "no" inputs have a minimum sensitivity of 1,5 V, but at proper setting, pulses of 0,5 V are effective.

If necessary, output pulses can be clipped to less than 5 ns wide pulses. Output pulses are 18 mA current pulses fed from a high impedance.

The circuit has an intrinsic threshold and incoming pulses need not to be previously limited.

The circuit has large rejection ratios, also for positive pulses due to its intrinsic limiting properties⁽³⁾.

The important feature, for resolving time considerations, is only in the amplitudes of input pulses. 1 V, 4 ns pulses are recommended inputs.

Clipping stubs are recommended with inputs directly connected to photomultipliers.

CIRCUITRY

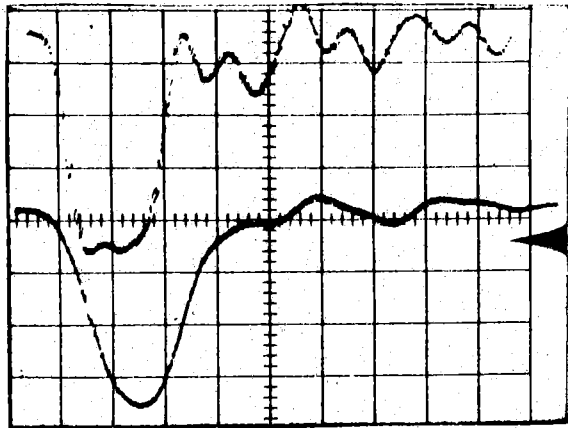
The basic ideas for the circuit are: the use of longtail-pairs as current switching devices and input buffers and the use of Schmitt active threshold to get the output amplitude and shape independent of input rise-time.

The latter is realized with a tunnel-diode discriminator in accordance to the ideas by Sugarman and others⁽³⁾.

The input transistor is reverse-biased of 0,3 V or more and the second one of the long-tail-pair is conducting current, remaining in its active region, through the tunnel diode, that is so biased on its low voltage state. Total current through the diode is the sum of the four input long-tail-pairs minus the peak-point current of the diode (e. g. 20 mA). When all yes input pulses are present, the reverse region current of the tunnel-diode reduces to zero so that the polarization in direct sense can act, firing the diode to its high voltage state. A current is so switched in the output transistor.

Long-tail-pairs act at the input as limiting buffer stages⁽⁴⁾. Besides they have the following advantages:

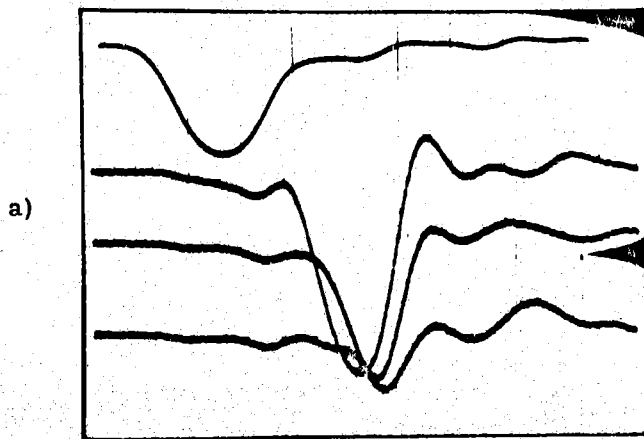
- 1) They provide a perfect buffer action between input pulses and output, also for capacity consideration. In fact a transistor of the long-tail-pair is perfectly cut-off when the input yes is present. We have had no problems in passing from the two-fold coincidence circuit to the four-fold one, and we think that it is easy to increase the number of yes inputs.
- 2) Input can be easily adopted to have a minimum reactive and ohmic mismatch.
- 3) The circuit is normally biased in an insensitive condition and has large factors of built in noise rejection. Moreover the circuit contains no critical parts.
- 4) The circuit has a very large rejection factor of temperature disturbances. Factors of $5 \cdot 10^{-5}$ for temperature variation from 0°C to 50°C are easily obtained.
- 5) The circuit allows to derive anticoincidence pulse without any change in the components, directly from coincidence input. No time overlapping is required and no delays are introduced.
- 6) The coincidence curves for several decreasing input voltages are contained one within the other, the external one having a time resolution of the same order the input pulses base width.



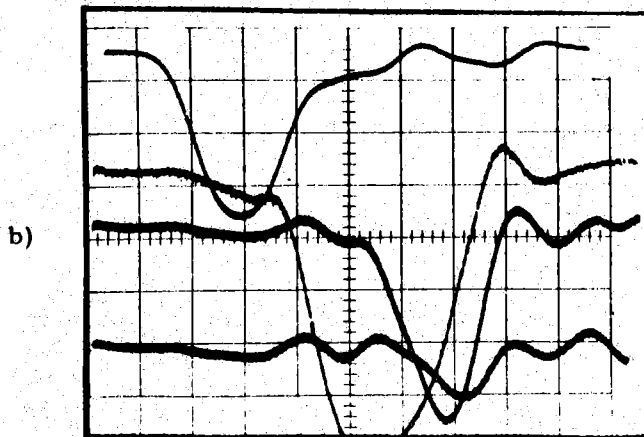
Horiz. 1 ns/cm Vert. 0.2 V/cm

FIG. 2 - Reflection tests at yes inputs.

- a) Voltage input pulse directly into 50 ohm sampling scope;
- b) Voltage input pulse with the circuit inserted there is less than 10% reactive mismatch.



- a. Input
- b. Output (coincidence)
- c. Output (1 ns delay)
- d. Output (1.5 ns delay)



Horiz. 1 ns/cm Vert. a. 1 V/cm
b. c. d. 0.2 V/cm

- a. Input
- b. Output (coincidence)
- c. Output (2 ns delay)
- d. Output (4 ns delay)

FIG. 3 - Output waveforms for input pulse width of 2 ns.

- a) for input pulses of 1.5 V;
- b) for input pulses of 3 VA.

Fig. 2 shows the reflection tests at yes inputs.

Fig. 3 shows the 18 mA coincidence pulses and output pulses obtained for delays of half and one time the incoming pulse width and for two different input voltages.

Fig. 4 shows the output amplitude Vs delay, taking the input voltages as a parameter. We can see that the resolving time decreases with input voltages. With input pulses, the larger than 1,5 V long-tail-pair switches with the same rise time (about 1 ns).

Fig. 5 shows experimental coincidence resolution time curves.

We can note no difference between time resolution for input pulses of 1.5 V and 5 V. The delay on the resolving time curve for incoming pulses larger than 2 times the minimum, is less than 2 ns to reduce the output pulse amplitude from 90% to 10%.

The property of intrinsic discrimination threshold can be of interest in many cases. Then we are interested to know what is the real threshold level as a function of input pulse widths. Some measurements appear in Fig. 6 with the input always referred to the earth and taking as a parameter the static current in the long-tail-pair.

LINEAR GATE

The circuit accepts negative current pulses from 1 mA to 20 mA linearly transferring them to the output cable fed from a high impedance source. Linearity is at least 1%, and the attenuation for the signal transfer is about 1,4 db. a. c. and d. c. pedestals are less than 1 mA. Rejection factor for non gated pulses is better than 20. The circuit has self limiting properties, being possible a sharp cut-off of incoming current pulses, when they are gated.

In fact we take advantage of the unilaterality of the gate diode and the output transistor forming a limiting circuit in which both contribute to the sharp cut-off, being driven through their non conducting region.

The gate pulse width may be chosen by changing a cable on the front panel, e. g. 6 ns, 10 ns, 20 ns.

For the circuit this correspond simply to the change of the cable length of the gating pulse generator.

Both input and output are referred to earth and so does the input for the trigger pulse of the gate-pulse generator. All are 50 Ω matched.

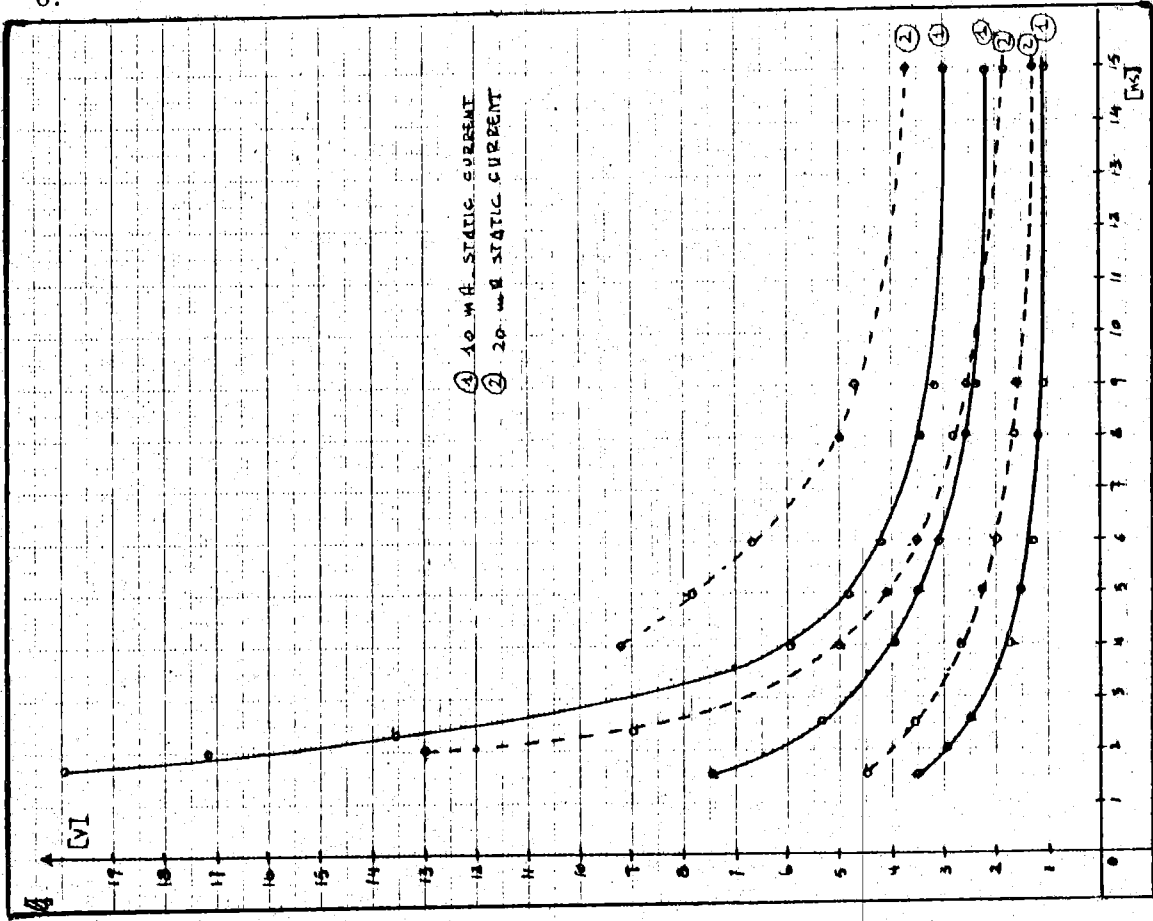


FIG. 6 - Input voltage at yes inputs Vs pulse width. 1. - 10 mA static current; 2. - 20 mA static current.

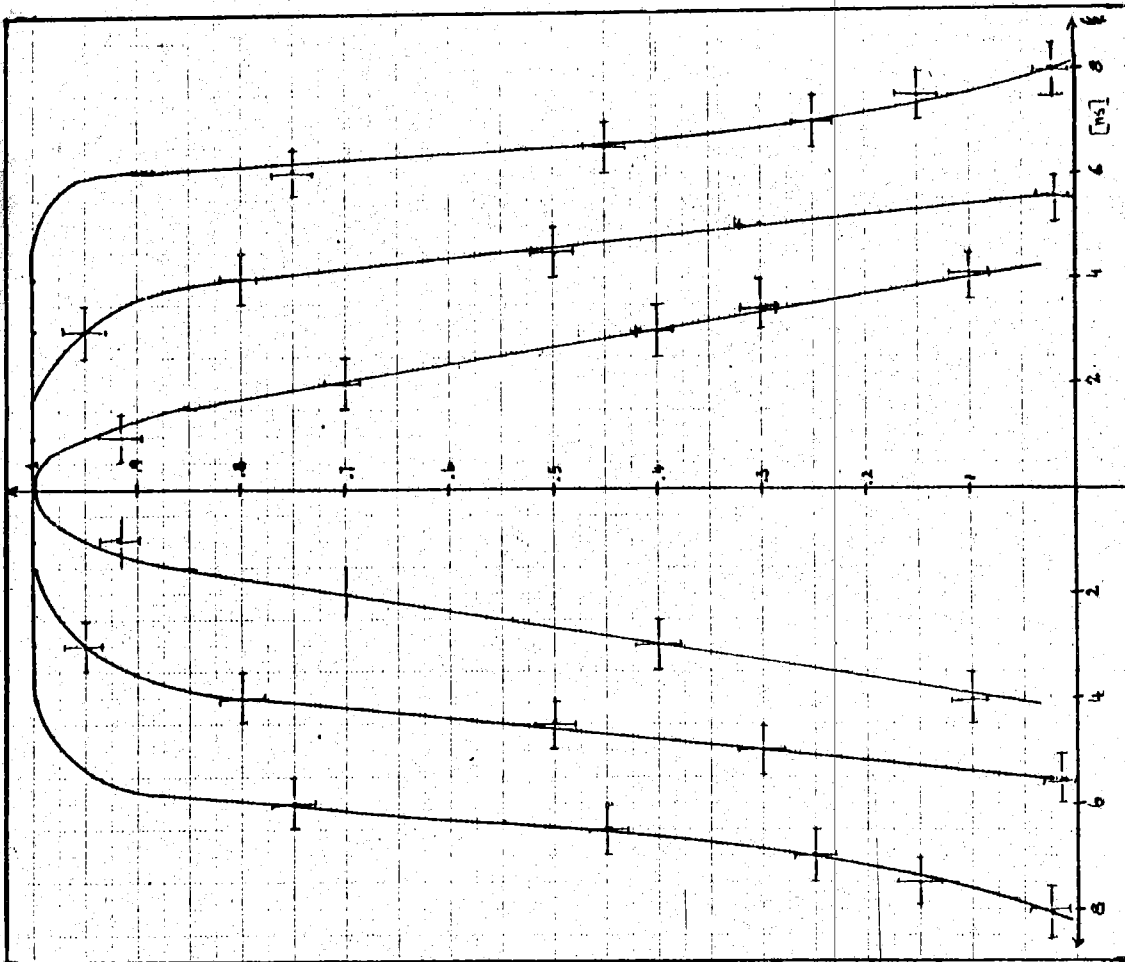


FIG. 4 - Coincidence circuit output amplitude Vs delay curves. 1. - 1.2 V input pulses; 2. - 2.5 V input pulses.

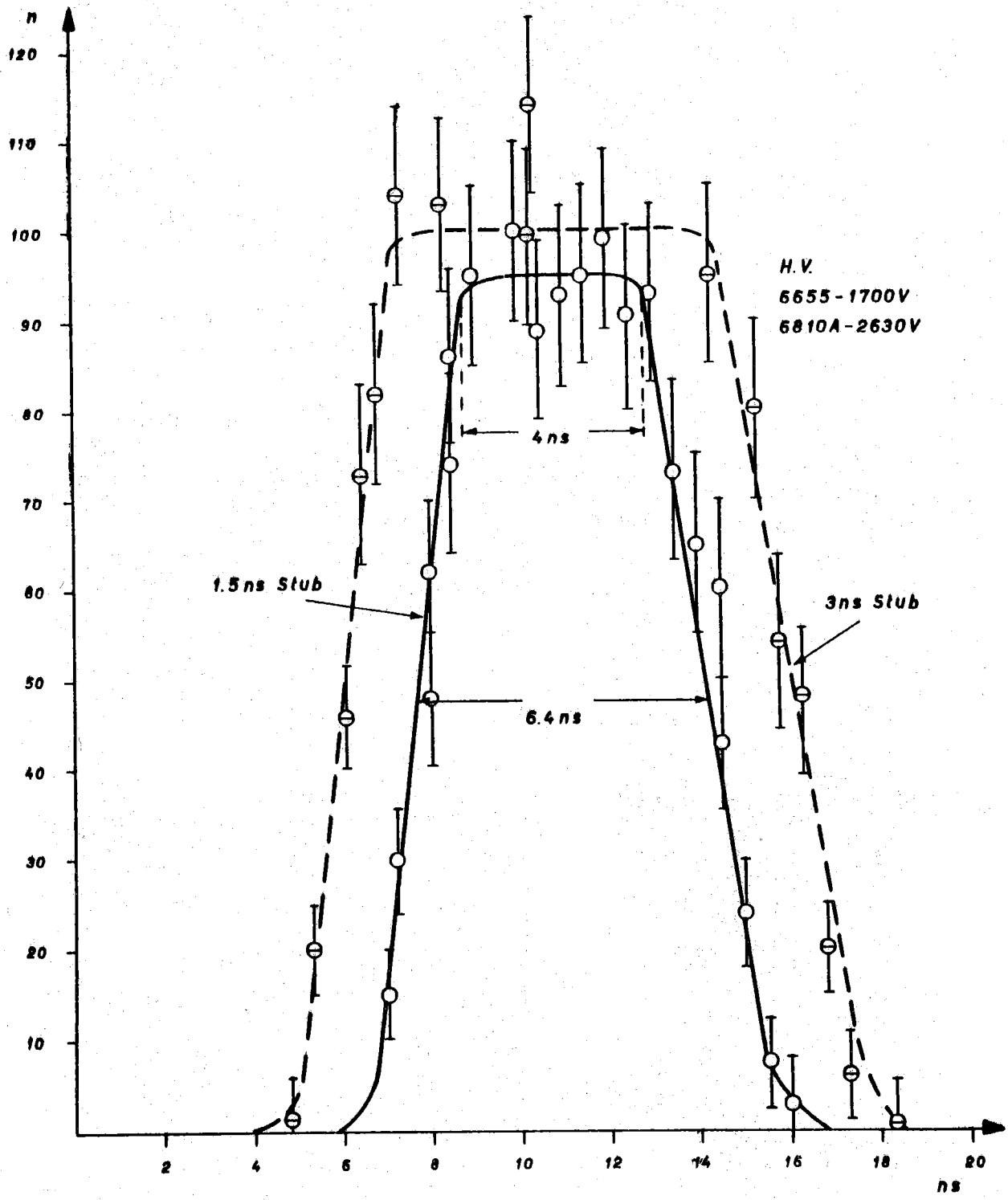


FIG. 5 - Resolving time curves obtained with photomultipliers 6810A and 6655 working on cosmic rays for two different width forming cables.

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The gate can be introduced in any point of the complete measuring chain.

THE CIRCUIT

The basic idea is to create a base-grounded complementary way to incoming current pulses, in series to which a diode is switched from its high to its low dynamic resistance region. The complete schematic is in Fig. 7.

The command to the diode is a forward current reduced by the incoming pulses. The command to the diode must then be a little larger than the incoming pulse.

The current way for the pulses is formed by the input transistor that is driving its current statistically remaining in the active region, and the output transistor that is nearly on. Between them a diode gate receives the command from a long-tail-pair current switch.

The 20 mA gating pulse generator is formed by a tunnel diode fed-back through a base-grounded transistor followed by a delay-line. This sets the pulse width and inverts the polarity to fire back the tunnel diode. Some provisions are kept to insure low voltage state static position for the tunnel diode. A d. c. collector base feed-back of the transistor will provide for stabilization. Rise and fall times are better than 1 ns.

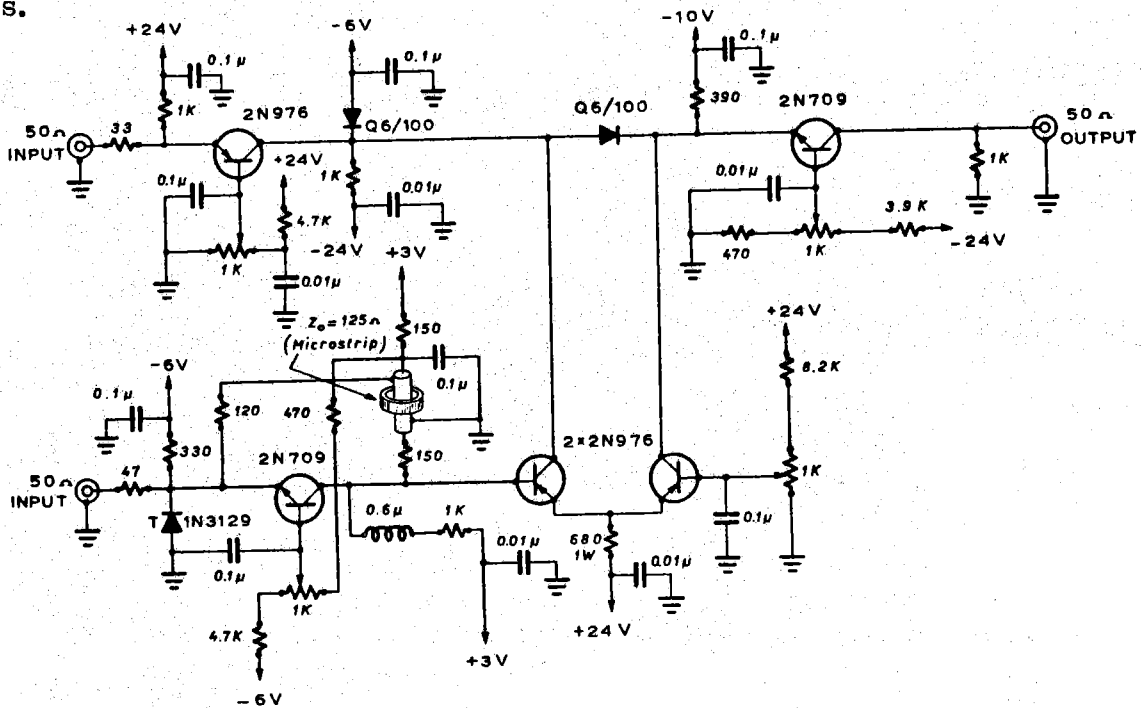
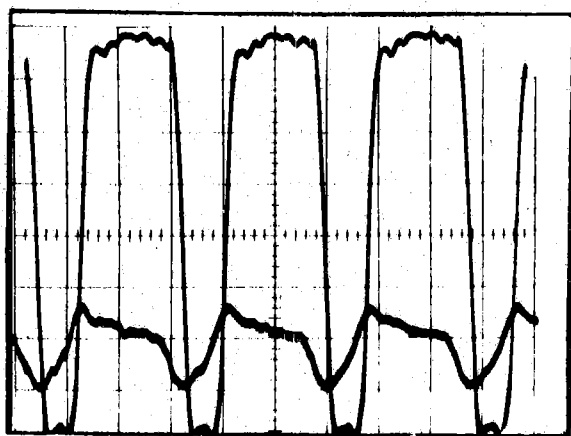
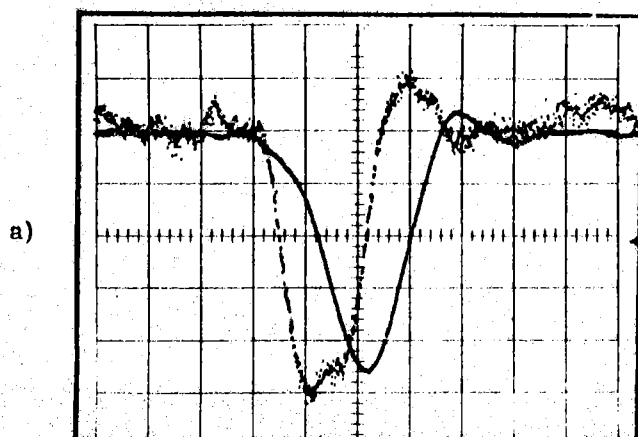


FIG. 8 - Complete circuit schematic of the Linear Gate.



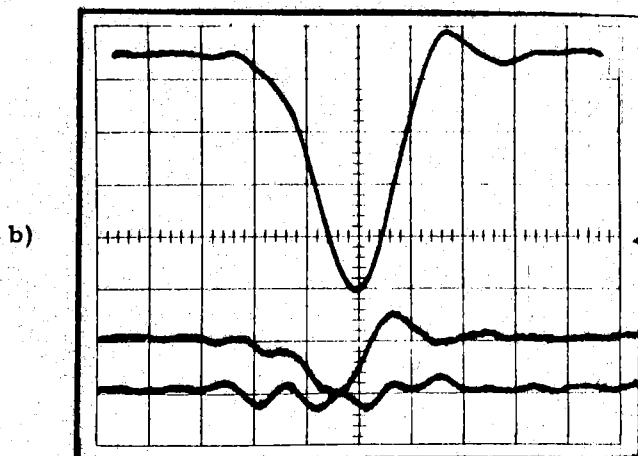
a) Horiz. 5 ns/cm Vert. 0.2 V/cm
 b) Horiz. 5 ns/cm Vert. 0.1 V/cm

FIG. 7 - Output waveforms of the gate pulse generator at 70 MHz.



Input pulse
 Output pulse

Horiz. 2 ns/cm
 Vert. 0.2 ns/cm



a. Coincidence between Gate and Input

b. With delayed gating pulse
 c. Without gating pulse

Horiz. 2 ns/cm Vert. a. 0.2 V/cm
 b. c. 0.05 V/cm

FIG. 9 - Input and output waveforms for 20 mA.
 a) without gating pulse;
 b) with a gating pulse, 6 ns wide.

Fig. 8 shows 70 MHz output waveforms of the generator.

We can report for the long-tail-pair current switch what observed for the coincidence circuit. Input and output wave-forms of the circuit for 20 mA pulses without gating pulse and with 6 ns width gating pulse, are shown in Fig. 9

Real gating time is the result of gate generator pulse shape and long-tail-pair rise time.

A measurement has been done with coincidence technique giving the results shown in Fig. 10 for a 6 ns and a 10 ns width gating pulse.

Moreover Fig. 9b shows the a. c. pedestal with and without the gating pulse.

Linearity of pulses transfer through the circuit is shown in Fig. 11.

Recently the gate diode has been substituted with a four-diodes sampling bridge⁽⁵⁾. This provides a simple way to the pulses of both positive and negative polarities, feeding them directly to the output.

ACKNOWLEDGEMENTS

We wish to thank Dr. A. Serra for useful discussion and for cooperation during the design and the laboratory tests of the circuits and during the preparation of the paper.

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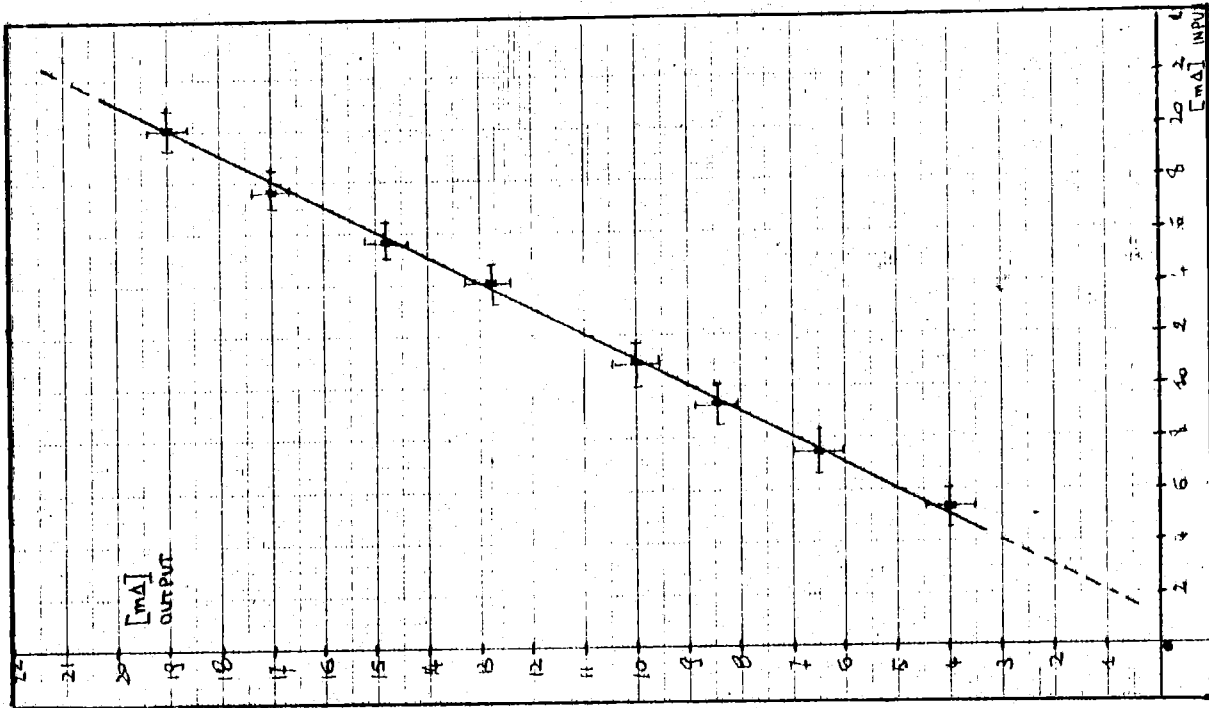


FIG. 11 - Linearity of current pulses transfer through the circuit.

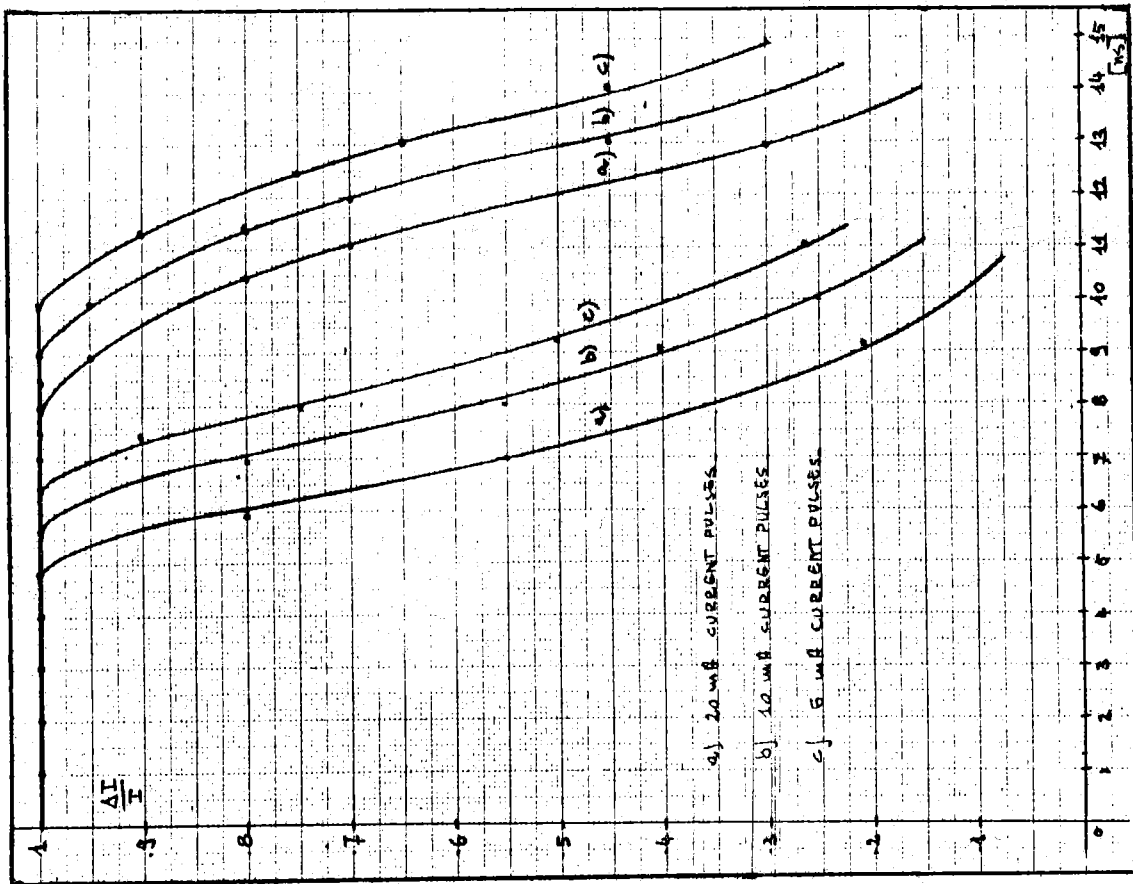


FIG. 10 - Output pulse amplitude relative to input Vs delay of gating pulse trigger.